| Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary) | ATTY. DKT. NO. 5181-62800<br>APPLICANT: Novak<br>FILING DATE: June 19, 2000 | SERIAL NO. 09/596,863<br>GROUP: ~~2836~~ 2817 |
|---|---|---|



| | | OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) |
|---|---|---|
| | B20 | Fang et al., "Modeling of the Electrical Performance of the Power and Ground Supply for a PC Microprocessor on a Card," © 1998 IEEE, pp. 116-119. |
| | B21 | Shi et al., "An Experimental Procedure for Characterizing Interconnects to the DC Power Bus on a Multilayer Printed Circuit Board," IEEE Transactions on Electromagnetic Compatibility, Vol. 39, No. 4, November 1997, pp. 279-285. |
| | B22 | Van den Berghe et al., "Study of the Ground Bounce caused by Power Plane Resonances," IEEE Transactions on Electromagnetic Compatibility, Vol. 40, No. 2, May 1998, pp. 111-119. |
| | B23 | Moran et al., "Application of the Finite-Difference Time-Domain Method and Measurement of Split Ground Plane Structures in Mixed Signal Integrated Circuits and Packages," May 1999, 2 pgs. |
| | B24 | Lescot et al., "Effect of a Metallic Ground Plane on Advanced CMOS On-Chip Interconnects," May 1999, 2 pgs. |
| | B25 | Novak, "Probes and Setup for Measuring Power-Plane Impedances with Vector Network Analyzer," February 1999, pp. 201-214. |
| | B26 | Daniele et al., "Spectral complete model for considering the effects of a finite ground plane on a PCB," 1996, pp. 226-229. |
| | B27 | Leroux et al., "Modelling of Power Planes for Electrical Simulations," 1996, pp. 664-668. |
| | B28 | Cai et al., "Numerical Extraction of Partial Inductance of Package Reference (Power/Ground) Planes," © 1995 IEEE, pp. 12-15. |
| | B29 | Young, "Case Study of Ground Plane Inductance and Implications for Simulation," ," IEEE Transactions on Components, Packaging, and Manufacturing Technology--Part B., Vol. 18, No. 1, February 1995, pp. 174-178. |
| | B30 | Peng, "Theory of Wave Guiding by Two-Dimensionally Periodic Structures: Progresses and Challenges," August 1999, 1 pg. |
| | B31 | Kelly et al., "Band Diagram for a Grounded Periodic Dielectric Substrate with Square Lattice and Finite Height," August 1999, 1 pg. |
| | B32 | Yang et al., "Fundamental Artificial-Periodic Substrate Effects on Printed Circuit Antennas," August 1999, 1 pg. |
| | B33 | Tzuang et al., "Guiding and Leaky Characteristics of Microstrip above Perforated Ground Plane," August 1999, 1 pg. |
| | B34 | Amari et al., "Simple Rules for Truncation of Periodic Structures to Achieve a Prescribed Bandcap Attenuation Level," August 1999, 1pg. |

EXAMINER: J Butler DATE CONSIDERED: 10-1-01

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

| Form PTO-1449 (modified)<br>List of Patents and Publications<br>For Applicant's Information<br>Disclosure Statement<br>(Use several sheets if necessary) | ATTY. DKT. NO. 5181-62800<br><br>APPLICANT: Novak<br><br>FILING DATE: June 19, 2000 | SERIAL NO. 09/596,863<br>2817<br>GROUP: ~~2836~~ |
|---|---|---|

OIPE
JUN 11 2001
PATENT & TRADEMARK OFFICE

| | | OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) |
|---|---|---|
| | B1 | Pannala et al., "Contribution of Resonance to Ground Bounce in Lossy Thin Film Planes," © 1998 IEEE, pp. 185-188. |
| | B2 | Libous, "Characterization of Flip-Chip CMOS ASIC Simultaneous Switching Noise on Multilayer Organic and Ceramic BGA/CGA Packages," © 1998 IEEE, pp. 191-194. |
| | B3 | Chen et al., "Norton Equivalent Modeling of Microprocessor Core Noise from Measurements," © 1998 IEEE, pp. 195-198. |
| | B4 | Kim et al., "Rejection of SSN Coupling in Multilayer PCB using a Conductive Layer," ~~© 1998 IEEE,~~ 1998 pp. 199-202. ~~IEEE Transactions~~ IEEE |
| | B5 | Becker et al., "Modeling, Simulation, and Measurement of Mid-Frequency Simultaneous Switching Noise in Computer Systems," IEEE Transactions on Components, Packaging, and Manufacturing Technology--Part B., Vol. 21, No. 2, May 1998, pp. 157-163. |
| | B6 | Huber et al., "Time-Domain Investigation of Decoupling Capacitors on MCM," May 1999, 2 pgs. |
| | B7 | Madou et al., "Electrical Characterisation of Capacitors Integrated in Multi-layer Printed Circuit Boards," May 1999, 2 pgs. |
| | B8 | Pham et al., "Decoupling Capacitors Techniques for High Frequency Board Designs," February 1999, pp. 127-135. |
| | B9 | Fisher et al., "The Role of Capacitors in High-Speed Systems Design," February 1999, pp. 137-155. High performance design Conference |
| | B10 | Lipa et al., "Flip-Chip Power Distribution," © 1998 IEEE, pp. 39-41. |
| | B11 | Wu et al., "Accurate Power Supply and Ground Plane Pair Models," © 1998 IEEE, pp. 163-166. |
| | B12 | Moll et al., "Extraction of Equivalent Circuit Models of Package Power Supply Distribution Systems from Full Wave EM Field Simulations," © 1998 IEEE, pp. 167-170. |
| | B13 | Fan et al., "Incorporating Vertical Discontinuities in Power-Bus Modeling using a Mixed-Potential Integral Equation and Circuit Extraction Formulation," © 1998 IEEE, pp. 171-174. |
| | B14 | Zhao et al., "Effects of Power/Ground via Distribution on the Power/Ground Performance of C4/BGA Packages," © 1998 IEEE, pp. 177-180. |
| | B15 | Novak, "Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination," © 1998 IEEE, pp. 181-184. |
| | B16 | Herrell et al., "Modeling of Power Distribution Systems in PCs," © 1998 IEEE, pp. 159-162. |
| | B17 | Chen et al., "Modeling and Simulation of Thin Film Decoupling Capacitors," © 1998 IEEE, pp. 205-208. |
| | B18 | Diaz-Alvarez et al., "Power Decoupling with Integral Capacitors and Area Array Connections," © 1998 IEEE, pp. 209-212. |
| | B19 | Roy et al., "ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications," © 1998 IEEE, pp. 213-216. |

EXAMINER: J Bolla DATE CONSIDERED: 10-1-01

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

| Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary) | ATTY. DOCKET NO: 5181-62800<br>APPLICANT: Novak<br>FILING DATE: June 19, 2000 | SERIAL NO: 09/596,863<br>GROUP: 2836 2817 |
|---|---|---|



## U.S. PATENT DOCUMENTS

| EXAM. INITIALS | REF. DES. | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE IF APPROPRIATE |
|---|---|---|---|---|---|---|---|
| | A1 | 3,209,284 | 9/1965 | Hast | 333 | 22RX | |
| | A2 | 3,678,417 | 7/1972 | Ragan et al. | 333 | 22R | |
| | A3 | 4,371,746 | 2/1983 | Pepper, Jr. | 178 | 18 | |
| | A4 | 4,626,889 | 12/1986 | Yamamoto et al. | 333 | 22RX | |
| | A5 | 5,114,912 | 5/1992 | Benz | 505 | 1 | |
| | A6 | 5,266,036 | 11/1993 | Lichtenwalter et al. | 439 | 65 | |
| | A7 | 5,523,727 | 6/1996 | Shingyoji | 333 | 22R | |
| | A8 | 5,670,917 | 9/1997 | Mazzochette | 333 | 22R | |
| | A9 | 5,708,400 | 1/1998 | Morris | 333 | 1 | |
| | A10 | 5,818,315 | 10/1998 | Moongilan | 333 | 2.38 | |
| | A11 | 6,104,258 | 8/2000 | Novak | 333 | 22R | |



## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|---|---|---|
| | A12 | Patent Abstracts of Japan, publication no. 05335812, published December 17, 1993. |
| | A13 | Patent Abstracts of Japan, publication no. 05055813, published March 5, 1993. |
| | A14 | Patent Abstracts of Japan, publication no. 05145306, published June 11, 1993. |
| | A15 | Abstract for SU 433 898, published October 30, 1982. |
| | A16 | Lei et al., "Power Distribution Noise Suppression Using Transmission Line Termination Techniques," © 1996 IEEE, pp. 100-102. |
| | A17 | O'Sullivan et al., "Developing a Decoupling Methodology with SPICE for Multilayer Printed Circuit Boards," © 1998 IEEE, pp. 652-655. |
| | A18 | Bandyopadhyay et al., "Importance of Damping and Resonance in Thin-Film Integrated Decoupling Capacitor Design," © 1997 IEEE, pp. 31-34. |
| | A19 | Fang et al., "Effects of Losses in Power and Ground Planes in the Simulation of Simultaneous Switching Noise," Proceedings of the 3rd Topical Meeting on Electrical Performance of Electronic Packaging, 1994 pp. 110-112. |
| | A20 | Franz et al., "An Approach to Determine Decoupling Effects of VCC and VCG Structures in Multilayer Technique," Proceedings of the 1994 EMC Symposium, May 1994, pp. 56-59. |
| | A21 | Ramo et al., Fields and Waves in Communication Electronics, Third Edition, John Wiley & Sons, Inc., 1994, Chapter 9, pp. 464-467. |
| | A22 | Lee et al., "Modeling and Analysis of Multichip Module Power Supply Planes," IEEE Transactions on Components, Packaging, and Manufacturing Technology--Part B, Vol. 18, No. 4, November 1995, pp. 628-639. |

EXAMINER: [signature] DATE CONSIDERED: 10-1-01

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.